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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/541,780
Filing Date: April 03, 2000
Appellant(s): NISHIMOTO, STEVE

Fred G. Pruner, Jr., (Reg. No. 40,779)
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the appeal brief filed on 24th of February 2003, and the reply brief filed on 12th of June 2003, as a supplemental examiner's answer based on the application 09/541,780 remanded to the Examiner by the Board (paper no. 17). The basis for the rejection has been restated to clarify the evidentiary support for the examiner's position.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 15-19

Claims 1-14 and 20-23 are allowed.

Upon reconsideration of the claim rejections in view of the appellant's arguments regarding claims 1-23. The Appellant's arguments regarding to the claims 1-14 and 20-23 in the brief filed on 24th of February, 2003 are persuasive. Therefore, the Examiner withdraws the claim rejections of the claims 1-14 and 20-23, and allows them.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows:

a. Can claims 15-19 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 15 ?

b. Can claim 16 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 16 ?

(7) Grouping of Claims

The rejection of claims 15-19 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

Applicant Admitted Prior Art in the Applicant's specification

6,049,883	Tjandrasuwita	4-2000
6,247,134	Sproch et al.	6-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Tjandrasuwita [US 6,049,883].

Fact Findings for Claim 15

Claimed Elements	AAPA's Facts
a) a system	a) a double pumped bus system in Fig. 2
b) double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data	b) several cells 12 and 14 may be serially coupled together to from a chain to relay data between the cells 14 using the double pumped technique in Fig. 2 (See page 3, lines 1-3)
	Tjandrasuwita's Facts
c) a circuit	c) latch circuit 502 of Fig. 5
d) said circuit to prevent communication of a data during a phase of clock signal	d) said latch circuit 502 to prevent communication of a serial data stream by disabling EN2 501 of

	the AND gate input (See col. 6, line 37) during a phase of clock signal, i.e., positive edge of Clock 406 in Fig. 5

Referring to claim 15, AAPA discloses a system (i.e., double pumped bus system in Fig. 2) comprising: double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data (See page 3, lines 1-3).

AAPA does not disclose at least one of said bus circuits being capable of being disabled to prevent bits from at least one of said sets of data from communicated through said at least of said bus circuits.

Tjandrasuwita discloses a clock gating apparatus, wherein a circuit (i.e., latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock gating apparatus, as disclosed by Tjandrasuwita, in said apparatus (i.e., double pumped bus system), as disclosed by AAPA, so as to allow said clock gating apparatus to enable or disable said double pumped bus circuits serially coupled together (i.e., the corresponding data path) as desired (See Tjandrasuwita, col. 3, lines 8-11) for the advantage of allowing power conservation (See Tjandrasuwita, Abstract).

Thus, AAPA, as modified by Tjandrasuwita, teaches at least one of said bus circuits being capable of being disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent bits from at least one of said sets of data (i.e., DATA 1 or DATA 2 in Fig. 1 of AAPA) from communicated through said at least of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita).

Fact Findings for Claim 17

Claimed Elements	AAPA's Facts
a) each double pumped circuit latches bits from one of said sets of data in response to first edges of a clock signal	a) each double pumped circuit latches bits using bit latches 16 and 18 in cell 12 from one of DATA 1 and DATA 2 in Fig. 1 in response to positive or negative edges of a clock signal

	(See page 2, lines 11-13)
b) said first edges being different from said second edges	b) a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal (See the prior art in the background of AAPA)

Referring to claim 17, AAPA discloses each double pumped circuit latches bits (i.e., latches bits using bit latches 16 and 18 in cell 12 of Fig. 1) from one of said sets of data (i.e., DATA 1 or DATA 2 in Fig. 1) in response to first edges (i.e., positive or negative edges) of a clock signal (See page 2, lines 11-13) and furnishes indications of said bits in response to second edges (i.e., negative or positive edges) of said clock signal (See page 2, lines 14-20), said first edges being different from said second edges (i.e., a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal; See the prior art in the background of AAPA).

Fact Findings for Claim 18

Claimed Elements	AAPA's Facts
a) said first edges in said system comprises positive edges of said clock signal	a) each double pumped circuit, i.e., latch 18 in cell 12 of Fig. 1, latches bits in response to the positive edges of a clock signal (See page 2, line 11)

Referring to claim 18, AAPA teaches said first edges in said system comprises positive edges of said clock signal (See page 2, line 11; i.e., each double pumped circuit (i.e., latch 18 in cell 12 of Fig. 1) latches bits in response to the positive edges of a clock signal).

Fact Findings for Claim 19

Claimed Elements	AAPA's Facts
a) said first edges in said system comprises negative edges of said clock signal under the condition of mutually exclusive	a) each double pumped circuit, i.e., latch 16 in cell 12 of Fig. 1, latches bits in response to the negative edges of a clock signal (See page 2, line 12)

Referring to claim 19, AAPA teaches said first edges in said system comprises negative edges of said clock signal under the condition of mutually exclusive application (See page 2, line 12; i.e., each double pumped circuit (i.e., latch 16 in cell 12 of Fig. 1) latches bits in response to the negative edges of a clock signal).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tjandrasuwita [US 6,049,883] as applied to claims 15 and 17-19 above, and further in view of Sproch et al. [US 6,247,134 B1; hereinafter Sproch].

Fact Findings for Claim 16

Claimed Elements	Tjandrasuwita's Facts
a) at least one of said double pumped circuits in said system are disabled to prevent said bits from at least one of said sets of data from being communicated through said at least one of said bus circuits	a) at least at least one of said double pumped circuits in said system, i.e., EN2 501 of the AND gate input in Fig. 5, are disabled to prevent said bits from at least one of said sets of serial data stream from being communicated through said EN2 of the AND gate input (See col. 6, lines 31-47)
	Sproch's Facts
a) alternate double pumped circuits in said system are disabled to prevent said bits.	a) a stall condition "C" determination circuit 210 of Fig. 8 and a stall signal propagation and clock gating circuit 230 of Fig. 3, i.e., D-latches and AND gates as combined in Fig. 8, alternately disable double pumped circuits, i.e., register latches 221,222,223,225 in Fig. 8, when the input operand bit streams are 110011001100... on DATA 1 on bus 242a and 001100110011... on DATA 2 on bus 242b in Fig. 8 (See col. 12, lines 48-51 for the alternate disabling condition of the clock gates 351,352,353 and 355 in Fig. 8)

Referring to claim 16, AAPA, as modified by Tjandrasuwita, discloses at least one of said double pumped circuits in said system are disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent said bits from at least one of said sets of data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) from being communicated through said at least one of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita).

AAPA, as modified by Tjandrasuwita, does not teach alternate double pumped circuits in said system are disabled.

Sproch discloses a method and system for pipe stage gating, wherein a stall condition "C" determination circuit 210 of Fig. 8 and a stall signal propagation and clock gating circuit 230 of Fig. 3 (i.e., D-latches and AND gates as combined in Fig. 8) alternately disable double pumped circuits (i.e., register latches 221,222,223,225 in Fig. 8) when the input operand bit streams are 110011001100... on DATA 1 on bus 242a and 001100110011... on DATA 2 on bus 242b in Fig. 8. Refer to col. 12, lines 48-51 for the alternate disabling condition of the clock gates 351,352,353 and 355 in Fig. 8.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus for alternately disabling said register latches, as disclosed by Sproch, in said embodiment of alternately disabling double pumped circuits, as disclosed by AAPA, as modified by Tjandrasuwita, for the advantage of further saving power in said double pumped bus when said bus does not care about said input data, e.g., its results are inconsequential because of equality (See Sproch, col. 3, line 64 through col. 4, line 3 and col. 12, lines 48-53).

(11) Response to Argument

In response to the Appellant's argument with respect to "Tjandrasuwita neither teaches nor suggests disabling a double pumped bus circuit from preventing bits from at least one of sets of data from being communicated through the disabled double pumped bus circuit", it is the Examiner's position that

Tjandrasuwita teaches a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Thereby, AAPA, as modified by Tjandrasuwita, teaches at least one of said bus circuits being capable of being disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent bits from at least one of said sets of data (i.e., DATA 1 or DATA 2 in Fig. 1 of AAPA) from communicated through said at least of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita). Furthermore, the Examiner believes that AAPA, as modified by Tjandrasuwita, discloses all the limitations of the Appellant's claim 15 with rationale for appropriate combination of the references because said clock gating circuit is well-known to one of the ordinary skill in the art of power saving control at the time the invention was made as shown by Tjandrasuwita at col. 2, lines 65-67. Further, Tjandrasuwita shows that the clock gating circuit could successfully control (i.e., allowing or preventing) said communication of said data from memory to mixer at Figure 5.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to "Background section of the application and Tjandrasuwita neither teach nor suggest that alternate double pumped bus circuits are disabled", the Examiner believes that the Appellant misinterprets the claim 16 rejection. In contrary to the Appellant's statement, the claim 16 is rejected under the ground of the rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tjandrasuwita and Sproch, not just AAPA in view of Tjandrasuwita, alone. The limitation "alternate double pumped bus circuits are disabled" is taught by Sproch in the combination of references applied in the prior rejections. In other words, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642

F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to "Sporach's disclosure does not teach or suggest the missing claim limitations, i.e., the disabling of alternate stages to prevent the communication of bits from a particular data flow" on the Reply Brief filed on 12th of June 2003, it is the Examiner's position that Sporach suggests the claimed limitation "the disabling of alternate stages to prevent the communication of bits from a particular data flow", such that a stall condition "C" determination circuit and a stall signal propagation/clock gating circuit alternately disable stages of double pumped circuits to prevent the communication of bits from a particular data flow 110011001100... on DATA 1 on the bus 242a and 001100110011... on DATA 2 on the bus 242b in Fig. 8, which is disclosed at col. 12, lines 48-51 for the alternate disabling condition of the clock gates 351,352,353 and 355 in Fig. 8.

Thus, Appellant's argument for this point cannot be seen as persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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